WHAT IS CLAIMED IS:

1. A half-rate clock and data recovery (CDR) circuit including a half-rate phase detector for detecting phases of an input signal and a half-rate clock, a charge pump circuit, a low-pass filter and a voltage controlled oscillator for feeding the half-rate clock back to the half-rate phase detector, the half-rate phase detector comprising:

first-stage and second-stage latch circuits;

further first-stage and second-stage latch circuits;

a selector circuit which receives an output of the first-stage latch circuit and an output of the further first-stage latch circuit so as to output a retimed signal;

a first exclusive OR circuit which receives an output of the second-stage latch circuit and an output of the further second-stage latch circuit so as to output a reference signal;

a latch delay circuit which is provided on a through-data path;

a one-pulse delay circuit which is provided on the through-data path so as to receive an output of the latch delay circuit and outputs through-data for generating a delay amount of one pulse; and

a second exclusive OR circuit which receives the retimed signal from the selector circuit and the through-data from the one-pulse delay circuit so as to output an output signal;

wherein phase comparison polarity of the half-rate phase detector provided with the one-pulse delay circuit enables use of an N type LC voltage controlled oscillator as the voltage controlled oscillator.

2. The half-rate CDR circuit according to Claim 1, wherein a gate size of

the one-pulse delay circuit of the half-rate phase detector is variable such that fine adjustment of the delay amount of one pulse in the one-pulse delay circuit can be performed.

3. The half-rate CDR circuit according to Claim 1, wherein a wiring length of the one-pulse delay circuit of the half-rate phase detector is variable such that fine adjustment of the delay amount of one pulse in the one-pulse delay circuit can be performed.

4. The half-rate CDR circuit according to Claim 1, wherein a plurality of pump-up bias circuits having different gate bias levels, respectively are provided for a pump-up constant current source of the charge pump circuit and a current quantity of the pump-up constant current source is changed upon changeover of the pump-up bias circuits such that fine adjustment of the delay amount of one pulse in the one-pulse delay circuit can be performed.

5. The half-rate CDR circuit according to Claim 1, wherein a plurality of pump-down bias circuits having different gate bias levels, respectively are provided for a pump-down constant current source of the charge pump circuit and a current quantity of the pump-down constant current source is changed upon changeover of the pump-up bias circuits such that fine adjustment of the delay amount of one pulse in the one-pulse delay circuit can be performed.

6. The half-rate CDR circuit according to Claim 1, wherein the number of pump-up constant current sources of the charge pump circuit is changed so as to change a current quantity of the pump-up constant current sources such that fine adjustment of the delay amount of one pulse in the one-pulse delay circuit can be performed.

7. The half-rate CDR circuit according to Claim 1, wherein the number

of pump-down constant current sources of the charge pump circuit is changed so as to change a current quantity of the pump-down constant current sources such that fine adjustment of the delay amount of one pulse in the one-pulse delay circuit can be performed.